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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,224	06/16/2005	Vincent Charles Venezia	BE02 0043 US	4536

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EXAMINER	
SINGAL, ANKUSH K	

ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/539,224	VENEZIA ET AL.	
	Examiner	Art Unit	
	Ankush k. Singal	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/16/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

`Arrangement of the Specification`

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The disclosure is objected to because of the following informalities: The applicant discloses on page3,line 32 "... polysilicon layer in the case of a silicon MOST...",The word MOST should be replaced by MOSFET.

Appropriate correction is required.

Claim Objections

Claim 1 objected to because of the following informalities: Claim 1,line 3 discloses "... method a semiconductor body..." which should be replaced by "forming a semiconductor body" instead of " method a semiconductor body" and "forming a source region" should be used instead of "method a source region" in claim 1,line 11.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2 and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu(US 6,348,390).

Re. claim 1, Wu discloses a method of manufacturing a semiconductor device with a field effect transistor in which:

Forming a semiconductor substrate(same as semiconductor body)(2) of a

semiconductor material is provided thereof, with a source region(27) and drain region (27) and with a gate region(16) between the source region and drain region, which gate region comprises a conductive layer(same as semiconductor region)(12) of a further semiconductor material that is separated from the surface of substrate(2)(same as semiconductor body)(as shown in figure below) by a gate insulating layer(same as gate dielectric)(10) , and with sidewall spacers(22)(same as spacer) adjacent to the gate region for forming the source and drain region(27)(Figure 5),

In forming the source region(27) and drain region(27) are provided with a metal layer(26) which is used to form a metal silicide layer(same as compound) of the metal and semiconductor material(column 5,line 54-58), and

The gate region(as shown above in the figure) is provided with a metal layer(26) which is used to form a metal silicide layer(same as compound) of the metal and semiconductor material(column 5,line 54-58), characterized in that before the spacers(22) are formed, a dielectric layer(same as sacrificial layer)(14) of a material that may be selectively etched with respect to the conductive layer(same as conductive layer) is deposited on the top of the conductive layer(12)(column 4, and line 44-48), and

After the sidewall spacer(22)(same as spacer) have been formed, the dielectric layer (same as sacrificial layer is removed(column 5,line 32-36), and
After the removal of the dielectric layer (same as sacrificial layer)(14) a metal layer(26) is deposited contacting the source ,drain and gate region (column 5,line 36-38).

Re. claim 2, Wu discloses having the sidewall spacers(same as spacers)(22) formed by depositing a layer of dielectric material on top of the substrate on which the gate region 16) comprising the conductive layer(12) and the dielectric layer(same as sacrificial region) (14) is present and by subsequently removing the deposited layer on top of and on both sides of the gate region by etching (Column 4,line 66-67 and column 5,line 1-13).

Re. claim 8, Wu discloses after the formation of the metal silicide layer(same as compound)(28) of the metal and semiconductor material(column 5,line 54-58), the spacers(22) are removed(Column 6,line 1-2).

Re. claim 9, Wu discloses semiconductor material chosen is silicon (column 3,line 34-36), and for the metal silicide layer(same as compound)(28) for the compound of the metal and the semiconductor material and the further semiconductor material a metal silicide is chosen(column 5,line 54-58).

Re. claim 10, Wu discloses a semiconductor device comprising a field effect transistor obtained by a method as claimed in any of the preceding claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35

U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu(US 6,348,390) in view of Hashimoto(US 2001/0003056).

Re. claim 3, Wu discloses all the limitations except having the semiconductor region completely consumed during the formation of the compound of the metal and the further semiconductor material.

However, Hashimoto discloses having gate electrode(120)(same as semiconductor region) completely consumed during the formation of the CoSi.sub.2 layer(same as compound)of the metal and the further semiconductor material(Para[0096],line 1-2).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wu as taught by Hashimoto to have the semiconductor region completely consumed during the formation of the compound of the metal and the further semiconductor material to minimizes the wiring resistance of the gate electrode (Para[0094],line 4-5).

Re. claim 4, Wu discloses all the limitations except the limitations disclosed in claim 4.

However, Hashimoto teaches the formation of the CoSi.sub.2 layer(same as compound) between the metal and the semiconductor material and the metal and the further semiconductor material is carried out in two separate heating steps, the first heating step resulting in an intermediate compound with a low content of the semiconductor material or of the further semiconductor material and in the second heating step the intermediate compound being converted to the compound having a higher content of the semiconductor material or of the further semiconductor material(Para[0096]).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wu as taught by Hashimoto to have the formation of compound with two step heating to have he surface portion of the Co.sub.2Si layer or CoSi layer prevented from being exposed during the high-temperature reaction and is therefore silicon-rich so that the surface energy of the Co.sub.2Si layer or CoSi layer is lower than in the conventional embodiment. As a result, agglomeration is less likely to occur at the surface of the Co.sub.2Si layer or CoSi layer so that a gate electrode composed of the CoSi.sub.2 layer with good uniformity in reaction thickness is formed(Para [0097].

Re. claims 5, Wu discloses all the limitations except the limitations disclosed in claim 5.

However, Hashimoto teaches that between the two heating steps, a part of the cobalt film (same as metal layer) which has not reacted to form the intermediate compound is removed by etching (Para [0073],line 6-9).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wu as taught by Hashimoto to have cobalt film (same as metal layer) which has not reacted to form the intermediate compound is removed by etching so that agglomeration is less likely to occur at the surface of the Co.sub.2Si layer or CoSi layer so that a gate electrode composed of the CoSi.sub.2 layer with good uniformity in reaction thickness is formed([Para[0097]).

Re. claim 6, Wu discloses all the limitations except the limitations disclosed in claim 6.

However, Hashimoto teaches having a silicon film(same as layer)of the further semiconductor material is deposited on the surface of the gate electrode(same as semiconductor body).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wu as taught by Hashimoto to have a layer deposited on the surface of the gate electrode to minimizes the wiring resistance of the gate electrode (Para[0094],line 4-5).

Re. claim 7, Wu discloses all the limitations except the limitations disclosed in claim 7.

However, Hashimoto teaches that after the second heating step, a part of the silicon film(same as layer)of the further semiconductor material which has not reacted to form the compound is removed by etching(Para[0080],line1-3).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wu as taught by Hashimoto a part of the silicon film(same as layer)of the further semiconductor material which has not reacted to form the compound is removed by etching to achieve a higher speed operation and low power consumption(Para[0089],line 15-16).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ankush k. Singal whose telephone number is 5712701204. The examiner can normally be reached on monday-friday 7am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MATTHEW SMITH can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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